UNIFIED DESIGN VERIFICATION FLOW FOR PRE-SILICON SOC POWER ESTIMATION AND ACHIEVING POST-SILICON CORRELATION TO CUSTOMER SAMPLING

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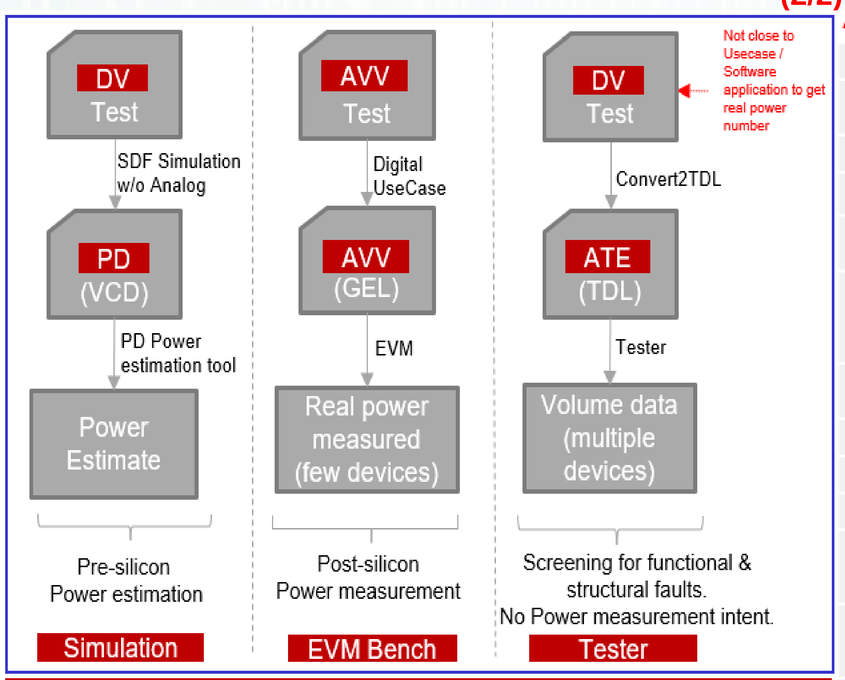
1. Motivation & Problem Statement (1/2)
SOC Power Estimation, Correlation and Customer Sampling

- Majority of semiconductor customers building applications on multi core designs with integrated RF work with **a power budget**.
- The SoC's power budget is decided during the architecture phase **based on empirical data which may vary at the end of Physical Design cycle**.
- After the SoC is fabricated, its **critical to correlate the Pre-SI and Post-SI power number** and identify range of power per block and **sample devices to customers** as per the power budget committed.
- SoC's real time power consumption number is decided by the Software code which can be developed at the end of design phase. So, currently there is no direct methodology to measure power on silicon at a large scale, unlike structural tests done on tester.
- This poster talks about the role of DV in the new methodology established for power correlation between Pre-SI estimates and Post-SI power measurement and how to screen devices on ATE to sample the right devices within the power budget limits.

2. Motivation & Problem Statement (2/2)



Problem Statement:
1. How to ensure pre-silicon and post-silicon power numbers are correlating by deciding on similar stimulus.
2. How to run UseCase on tester so that ATE screening ensures samples with right power budget reach customers.

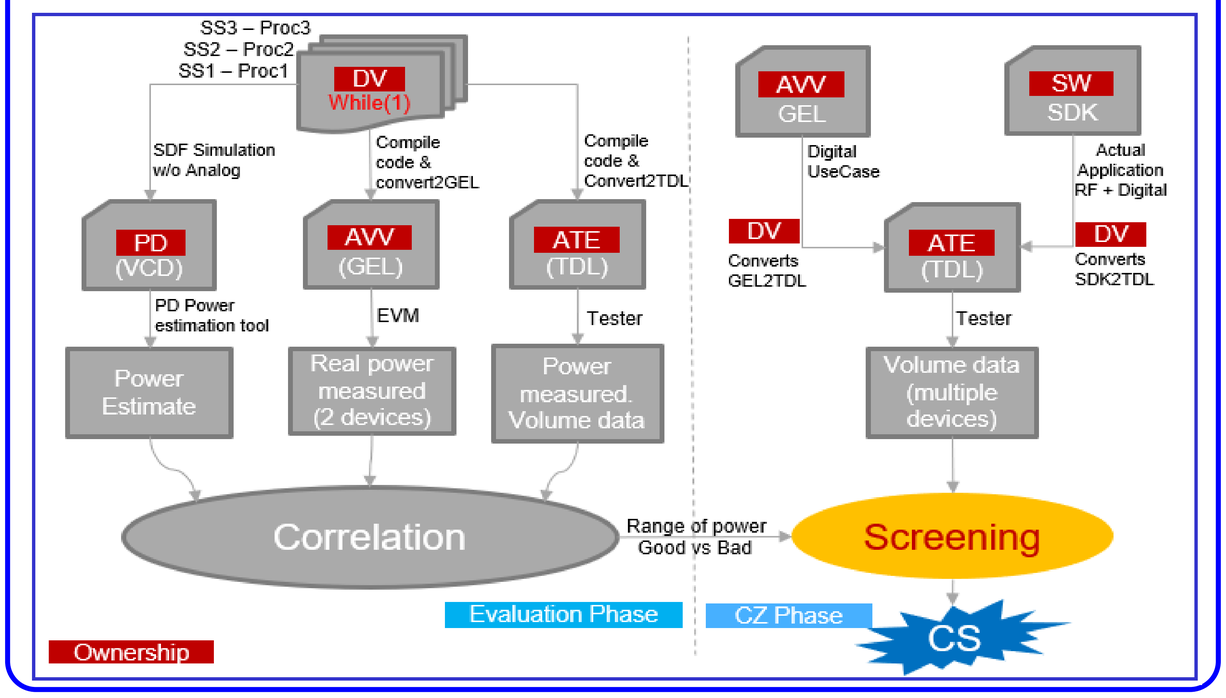
This could have been approached with porting UseCase from AVV suite to DV & dumping VCDs but it is significant effort in porting, also results in long run times of tests and dump sizes of VCD & analysis time on Voltus.

Abbreviations:

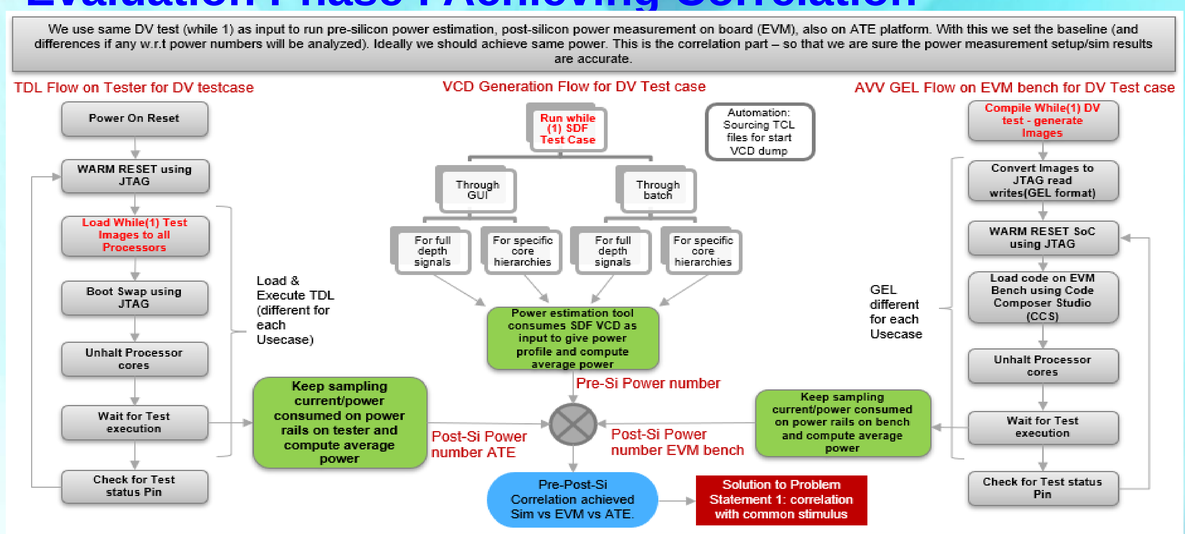
DV	Design Verification
AVV	Application Verification and Validation
PD	Physical Design
SDK	Software Development Kit
SS1/2/3	Sub-System 1/2/3 (Proc - Processor)
GEL	General Extension Language (Code format understood by code composer studio) for JTAG based read writes
VCD	Value Change Dump (toggle activity in simulation)
CZ	Characterization
ATE	Advanced Test Equipment
CS	Customer Sampling
EVM	Evaluation module (Has SoC package mounted on a PCB with JTAG connector)
TDL	Test Description Language (interpreted by tester and replayed on the SoC PADs in ATE)
SoC	System On Chip
SW	Software
SDF	Standard Delay Format

3. Proposed Solution (1/3)
Power Estimation – Correlation – Screening - CS

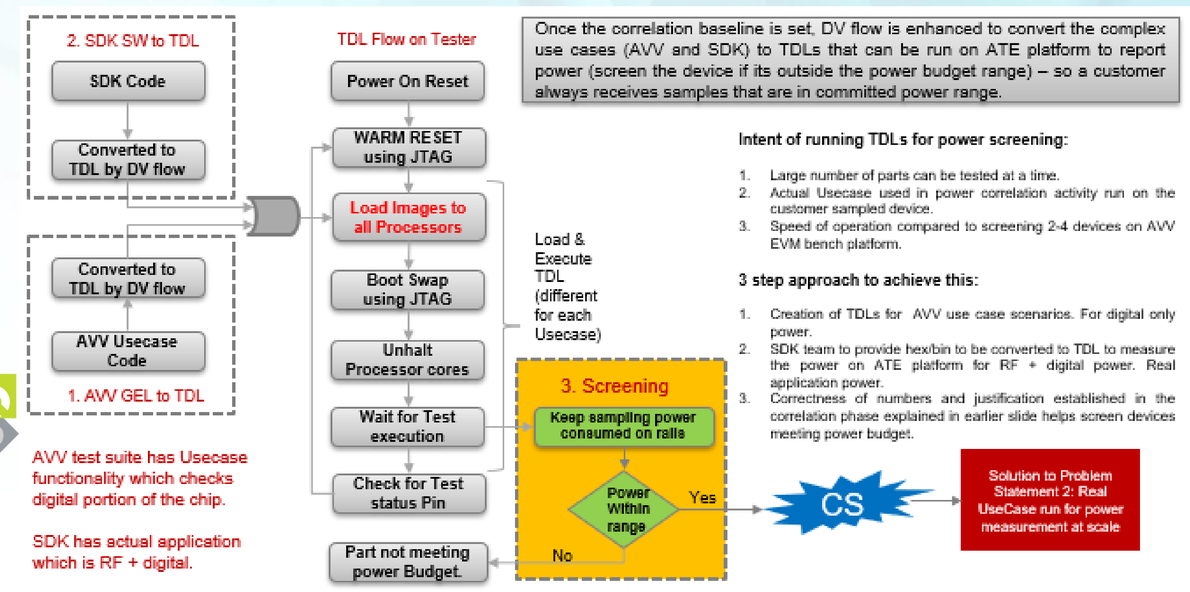
- Proposed DV framework establishes correlation between PD, EVM bench and ATE platform using common DV input stimulus and cuts down on power measurement and correlation effort to achieve deterministic Customer Sampling



4. Proposed Solution (2/3)
Evaluation Phase : Achieving Correlation

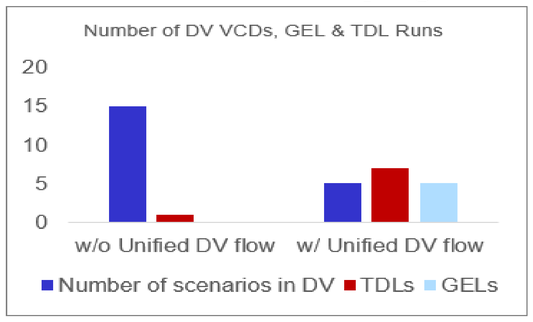


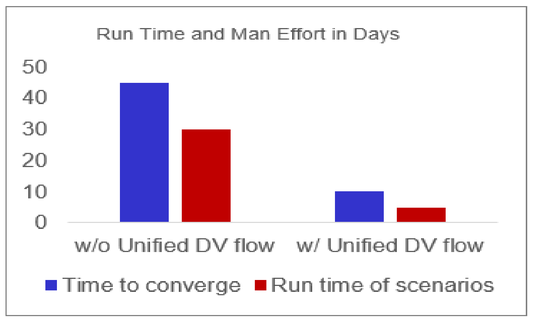
5. Proposed Solution (3/3)
CZ Phase : Screening and Customer Sampling (CS)



6. Evidence and Results

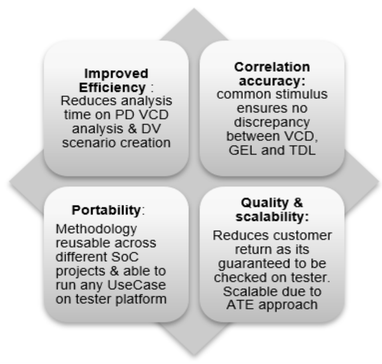
- We established correlation between PD, EVM bench and ATE platform using common DV input stimulus successfully in an ongoing project.
- Correlation ensures reduction in number of scenarios run, correctness of measurements between setups and overall efficiency improvement with re-use of AVV & SDK code.
- An automated flow is implemented to run AVV UseCase (GELs) and SDK code on ATE, thereby reducing VCD analysis effort in PD and complex DV test creation.
- Helps avoid DV testcase creation and runtime challenges.
- Also, with limited Analog modelling aspect we can not achieve accurate power number in simulation and hence overall methodology works well for power estimation, correlation and customer sampling at scale.





7. Conclusions

- Power estimation & correlation activity is streamlined with DV while(1) testcase as common input stimulus.
- At scale screening in CZ phase of devices prior to customer sampling is enabled avoiding customer returns on parts which result in high power consumption.
- Efficient and faster closure with minimal pre-silicon checks. Reduction in DV by leveraging AVV & SDK code and do it on the tester instead.



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